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SEMICONDUCTOR TECHNOLOGY PROGRAM

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ABSTRACT - This report provides information on the current status of NBS work on measurement technology for semiconductor materials, process control, and devices. Emphasis is placed on silicon and silicon-based devices. Highlighted activities include newly issued resistivity SRMs, characteristics of sulfur-related deep levels in silicon, photoluminescence of indium-doped silicon, effect of tertiary interferograms on Fourier transform spectroscopy, design information for a set of wafer optical linewidth standards, modeling of short-channel MOS transistors, acoustic-emission testing of tape-bonded ICs, laser scanning of a solar cell test pattern, power loss of transistor leads during fast switching, and second breakdown and radiation effects in power MOS transistors. Brief descriptions of an upcoming linewidth measurement seminar and a survey of Federal IC processing facilities are given. In addition, recent publications and publications in press are listed. The report is not meant to be exhaustive; contacts for obtaining further information are listed.

KEY WORDS - Electronics; integrated circuits; measurement technology; microelectronics; semiconductor devices; semiconductor materials; semiconductor process control; silicon.

Preface

This report covers results of work during the fifty-first quarter of the NBS Semiconductor Technology Program. This Program serves to focus NBS research on improved measurement technology for the use of the semiconductor device community in specifying materials, equipment, and devices in national and international commerce, and in monitoring and controlling device fabrication and assembly. This research leads to carefully evaluated, well-documented test procedures and associated technology which, when applied by the industry, are expected to contribute to higher yields, lower cost, and higher reliability of semiconductor devices and to provide a basis for controlled improvements in fabrication processes and device performance. By providing a common basis for the purchase specifications of government agencies, improved measurement technology also leads to greater economy in government procurement. Financial support of the Program is provided by a variety of Federal agencies. The sponsor of each technical project is identified at the end of each entry in accordance with the following code: 1. The Defense Advanced Research Projects Agency; 2. The National Bureau of Standards; 3. The Division of Electric Energy Systems, Department of Energy; 5. The Defense Nuclear Agency; 6. The C. S. Draper Laboratory; 10. The Naval Weapons Support Center; 11. The Solar Energy Research Institute; 12. The Naval Avionics Center; 13. The Lewis Research Center, National Aeronautics and Space Administration; and 15. The Naval Ocean Systems Center.

This report is provided to disseminate results rapidly to the semiconductor community. It is not meant to be complete; in particular, references to prior work either at NBS or elsewhere are omitted. The Program is a continuing one; the results and conclusions reported herein are subject to modification and refinement. Further information may be obtained by referring to more formal technical publications or directly from responsible staff members, telephone: (301) 921-listed extension. General information, past issues of progress briefs, and a list of publications may be obtained from the Electron Devices Division, National Bureau of Standards, Washington, D.C. 20234, telephone: (301) 921-3786.

Silicon Resistivity SRMs

A new silicon resistivity SRM is now available from the NBS Office of Standard Reference Materials (OSRM). This SRM, designated SRM 1523, Silicon Resistivity Standard for Eddy Current Testers, is designed primarily for use with "contactless" resistivity testers; it is also suitable for use with four-probe instruments. It contains two boron-doped silicon slices, one each at nominal resistivities of 0.01 and 1 Ω•cm. The slices are nominally 2 in. (51 mm) in diameter and 0.63 mm thick; they were cut from (100) Czochralski and (111) float-zone-grown crystals, respectively. The resistivity of each slice was individually measured by the four-probe technique using ASTM Method F 84. The 95-percent confidence level on the stated resistivity values is ±2.5 percent of those values. This confidence value is a conservative statement resulting from a two-instrument, two-operator experiment at NBS.

This SRM supplements the values of silicon resistivity standards which are available in two other previously announced SRMs. Supplies of these SRMs have recently been replenished; both are now available from the OSRM. SRM 1521 contains two slices of (111) float-zone-grown, boron-doped silicon at nominal resistivities of 0.1 and 10 Ω•cm. SRM 1522 contains three slices of (111) silicon doped with phosphorus by the neutron transmutation process to nominal resistivities of 25, 75, and 180 Ω•cm. All slices in SRM 1521 and SRM 1522 are also nominally 2 in. in diameter and 0.63 mm thick; each has been individually measured and certified.

The price for SRM 1523 is $300, and the prices for SRM 1521 and 1522 are $300 and $425, respectively. [Sponsor: 2]

(J. R. Ehrstein, x3625)

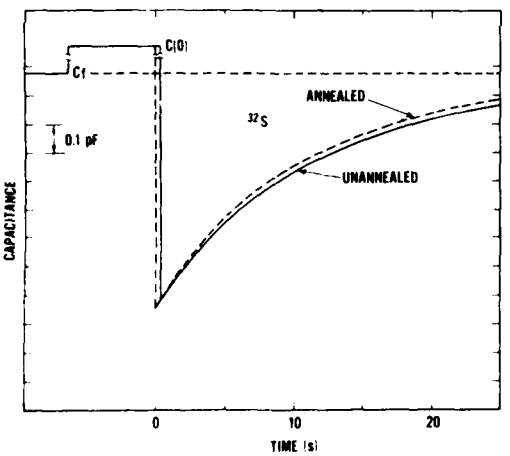
Deep-Level Measurements

Additional electrical evidence has been obtained which confirms the complex nature of sulfur-related deep levels in silicon. One would expect that the thermal emission rate from a single physical defect species in silicon would be a well-defined, reproducible function of the temperature of the test specimen. Examination of the effect of a variety of experimental factors on the thermal emission rate from sulfur-related centers in silicon revealed that the rate varies with virtually every experimental parameter studied.

Deep-level transient spectroscopy (DLTS) measurements were made on six silicon wafers into which sulfur had been introduced in varying amounts by ion implantation (and subsequent redistribution at 1000°C). At low sulfur density, the spectrum exhibits two sulfur-related peaks of about the same amplitude. As the sulfur density increases, the amplitude of the lower temperature peak increases more rapidly than that of the higher temperature peak. In addition, the positions of these peaks shift and other peaks appear in the spectrum. Differences from the spectra of these ion-implanted specimens are also observed in the DLTS spectrum of a silicon wafer into which the sulfur was introduced by diffusion in a sealed quartz tube at 1350°C.

More precise determination of the thermal emission rate is possible with the use of the isothermal transient capacitance (ITCAP) method. Differences, such as that illustrated in the accompanying figure, are observed in the time constant of the capacitance transient before and after a thermal anneal. The figure shows the capacitance of the depletion layer as a function of time, starting from before the trap-filling

phase of the measurement cycle, through the charging cycle when the depletion layer is collapsed by reducing the reverse-bias voltage and thereby drastically increasing the capacitance, and ending with the transient overshoot and recovery following restoration of the reverse-bias voltage to its initial value. Because annealing made a small change in the initial capacitance (from 136 pF to 126 pF), the post-anneal curve was translated vertically so that both curves coincide prior to the trap-filling phase. In addition to this vertical shift, the post-anneal curve was shifted horizontally to bring a point on its transient recovery curve into coincidence with the beginning of the transient recovery point on the pre-anneal curve in order to show more clearly the difference between the rates of transient recovery and thus the differences in emission rate (or reciprocal time constant) caused by annealing. Analysis of these curves reveals that, after anneal the time constant of recovery decreased, by about 14 percent, from 11.5 s to 9.9 s. Although this effect is rather small, it is a real effect that has been seen in all four specimens examined to date.



ITCAP transient responses at 129.95 K of the shallow sulfur-related center in an implanted specimen. Dashed curve: specimen annealed in an inert atmosphere for 5 h at 550°C. Solid curve: as-fabricated specimen.

Variation was also observed in the thermal emission rate from the deeper sulfur level at 204.9 K as a function of depth below the p-n junction test device using the ITCAP technique. This is the only successful demonstration of variability that involves a single unaltered specimen. The other demonstrations have involved different specimens, or a single specimen subjected to some form of heat treatment.

These variations in relative amplitudes and in apparent emission rates under different experimental conditions suggest that the emission is not coming from a single defect species but rather from a manifold of unresolved closely spaced levels whose relative composition varies in unknown and uncontrolled ways as previously suggested on the basis of measurements of the optical spectra. [Sponsors: 2,3] (R. D. Larrabee, W. E. Phillips, and W. R. Thurber, x3625)

Photoluminescence Studies

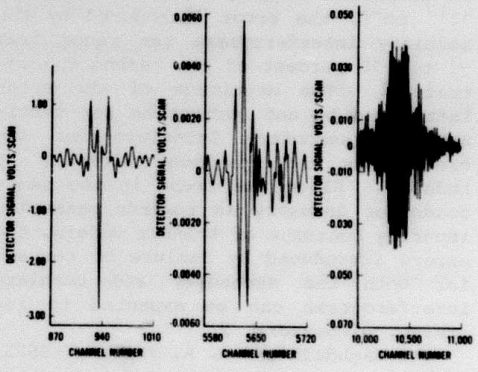
The photoluminescence spectrum of indium-doped silicon measured at 2 and 4 K using samples from several suppliers has been found to be preparation sensitive. Intensity variations enable one to distinguish a sharp no-phonon line at 1.118 eV, variously referred to as U_2 or P, and its associated vibronic spectrum from the In(NP) lines and their phonon replicas. Whereas the intensity of the latter did not show preparation sensitivity, the former changed by three orders of magnitude depending on the details of the surface preparation procedures. Although the reasons for the preparation sensitivity are not yet understood, it is possible to draw some conclusions regarding the nature of the U_2 spectrum. The U_2 vibronics form a broad-structured spectrum containing density-of-states features. The appearance of phonons other than those conserving crystal momentum demonstrates that the exciton is bound to a low sym-

metry site. In addition, the spectrum includes a peak at 1.109 eV and a shoulder at 1.107 eV which involve too small an energy loss to be density-of-states related; these features are most likely modes of the U_2 impurity complex. This complex has been tentatively identified as an isoelectronic center composed of an indium-phosphorus nearest-neighbor substitutional pair. [Sponsor: 2] (R. E. Stahlbush* and R. A. Forman, x3625)

Fourier Transform Spectroscopy

The recent increase in the use of Fourier transform spectrophotometers (FTS) for routine quantitative analysis of semiconductor wafers has led to a more careful examination of the experimental artifacts associated with these instruments. In FTS the most important instrumental difficulties affecting quantitative measurements are due to multiple passes. Imprecision can also occur due to the method of analysis of the interferogram, such as the choice of the apodization function, as well as to "ghost" spectra. In the analysis of the absorption spectra of thin solid samples, Fabry-Perot fringes present a complication for both dispersive and transform spectroscopy. These fringes are observed in FTS as secondary interferograms superimposed upon the main interferogram. These interferograms are due to internal reflections within the specimen, which result in additional phase delays for some portions of the radiation reaching the detector. In the case of dispersive spectroscopy, a computer can be used to remove the fringes by curve fitting. Alternative methods for removing the fringes include using an identical thickness reference specimen in a double-beam spectrophotometer, mounting the specimen at the Brewster's angle, using a wedge-shaped specimen to eliminate the fringes entirely, or using low resolution. In FTS, many of the geometric techniques are not as effective in removing fringes, because in this instrument the beam has a relatively large solid angle or "etendue." Thus, other methods which involve modifying the observed (untransformed) interferograms to eliminate these artifacts from the transformed spectrum have been developed and reported in the literature.

In experiments with silicon wafers which were highly polished on both surfaces, a series of tertiary interferograms as shown in the accompanying figure was observed in addition to the secondary interferograms. These interferograms were determined to be due to a combination of multiple reflections within the wafer and multiple reflections between the wafer and the Michelson interferometer. The amplitude of these tertiary interferograms depends on the actual reflectance of the wafer surfaces; typically it was weaker than the amplitude of the secondary interferograms roughly by a factor of six. This may introduce an error on the order of a few percent in the measurement of an impurity concentration in a polished silicon wafer of thickness comparable to that of wafers used for semiconductor device fabrication.



Sections of an interferogram of a 0.869-mm thick wafer, showing the relative magnitudes of the main (left), tertiary (center), and secondary (right) interferograms. Note the scale changes. The channel number is directly proportional to the mirror position with 1000 channel numbers approximately equal to 0.0633 mm.

*NBS-NRC Postdoctoral Research Associate.

A computational technique, such as that of Hirschfeld and Mantz which was developed to eliminate the effects of secondary interferograms, can also be applied to remove the effects of tertiary interferograms. In this technique, the interferometer signal is removed from the region in which the amplitude of the extraneous interferogram is greater than the amplitude of the main interferogram. The signal in this region is then replaced by the signal from this region of an interferogram obtained with a different specimen thickness.

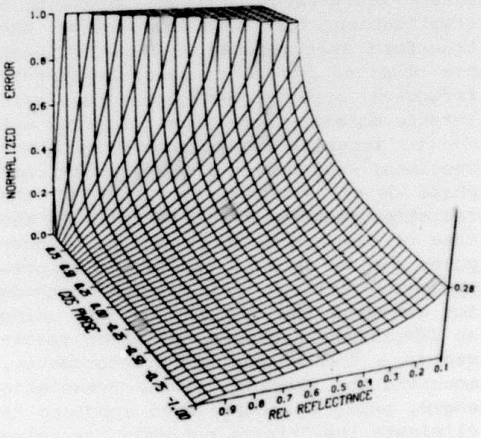
This procedure was applied in determining the carbon content of a 0.869-mm thick silicon wafer by measuring the intensity of the substitutional carbon absorption line at 607 cm^{-1} at room temperature. A high-purity 2.0-mm thick vacuum float-zoned wafer was used as a reference. The carbon density determined from a fully corrected interferogram was 1.256×10^{17} cm^{-3}. If the tertiary interferograms are not removed, the apparent carbon density is lower by 0.011×10^{17} cm^{-3}. Since Czochralski silicon wafers generally contain carbon in densities ranging from ~0.1 to ~1 × 10^{17} cm^{-3}, the error introduced by the tertiary interferograms can range from ~1 to ~10 percent of the carbon concentration. The magnitude of the error introduced by not correcting for tertiary and secondary interferograms increases as the specimen thickness is reduced. Since the trend in the semiconductor industry is towards measuring impurity contents of thinner wafers, the errors introduced by failure to correct for both the secondary and tertiary interferograms can be expected to increase. [Sponsor: 2]

(A. Baghdadi and R. A. Forman, x3625)

Optical Linewidth Measurements

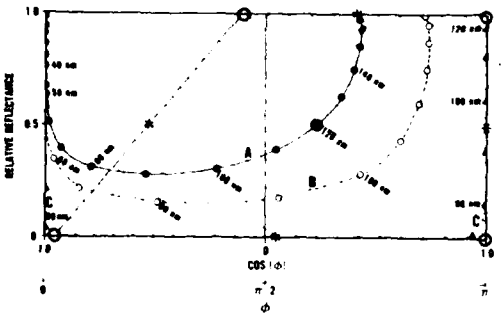
A preliminary design has been developed for an optical linewidth calibration artifact for calibrating systems for measuring patterns in a wide variety of materials found on IC wafers. Except for the details of the edge geometry, all patterned layers found on IC wafers can be characterized by two parameters. These parameters are the relative reflectance R_o or contrast at the edge and the optical phase difference ϕ_o. These parameters can be determined either by calculation from the Fresnel equations with appropriate normalization using known layer thicknesses and indices of refraction or by experimental measurement. The Fresnel equations yield accurate values only for monochromatic illumination near normal incidence, but these requirements are well approximated in practice if typical interference filters (100-nm bandpass) and illuminating N.A.'s of 0.20 or less (Köhler illumination) are used.

When linewidth measurements are made on low contrast lines using the center of the dark band along the line edge for edge detection, the resulting error in linewidth can be calculated for a diffraction-limited optical system as shown in the accompanying three-dimensional plot of the error surface. As indicated, the center of this dark band corresponds to the line edge (no



Three-dimensional plot of error surface. To convert normalized error to distance in micrometers, multiply by wavelength (in μm) and divide by the numerical aperture.

error) only along the axis where R_o = 1. As the contrast at the line edge increases (R_o < 1.0), the error in linewidth increases, scaling with wavelength of the illumination and inversely with the N.A. of the objective. Because of the predictable behavior of this known systematic error, it is possible to calibrate such a system using far fewer pairs of values of R_o and ϕ_o than would normally be required to characterize an unknown error surface. For the case illustrated, a third-order polynomial can be used for calibration, and only five combinations of R_o and ϕ_o are required to characterize the error surface. Some possible choices are shown in the accompanying plot of the R_o-ϕ_o plane. The optimum coordinates (R_m, ϕ_m) are determined by application of Gauss-quadrature formulas. These formulas have been developed for simple square and circular regions. Mapping of the known optimum coordinates for a square region onto the indicated trapezoid produces the families of points shown on the plot. Several of the points shown correspond to patterned single layers of oxide or nitride on silicon. Other pairs of R_m, ϕ_m values can be produced from a variety of materials if multilayer substrates are used.



View of the R_o, ϕ_o plane showing sets of points (set 1, ✱; set 2, O) which can be used to calibrate the shaded trapezoidal region. Curves correspond to layers with increasing indices of refraction: A) silicon dioxide on silicon (n = 1.46), B) nitrided SiO_2 on silicon (n = 1.6), and C) Si_3N_4 deposited by LPCVD (n = 1.98).

Plans are underway to fabricate such a set of wafer materials and test this method of calibration on commercially available linewidth measurement systems. For other edge-detection criteria, an optimum set of R_m, ϕ_m values may be similarly determined. [Sponsor: 2]

(D. Nyyssonen, x3621)

Linewidth Measurement Seminars

A 3-day training seminar on Linewidth Measurements on Integrated Circuit Photomasks and Wafers is to be held in the Washington, D.C. area on November 18-20, 1981, to present up-to-date information on the accurate measurement of linewidths in the 0.5- to 10-μm range. The seminar includes lecture sessions, equipment demonstrations, and group discussions. Emphasis is on optical microscope techniques. The 75-person capacity of this seminar is expected to be oversubscribed; a similar seminar is tentatively scheduled to be held in the Southwest in the fall of 1982. [Sponsor: 2] (E. C. Cohen, x3786, and J. M. Jerke, x3621)

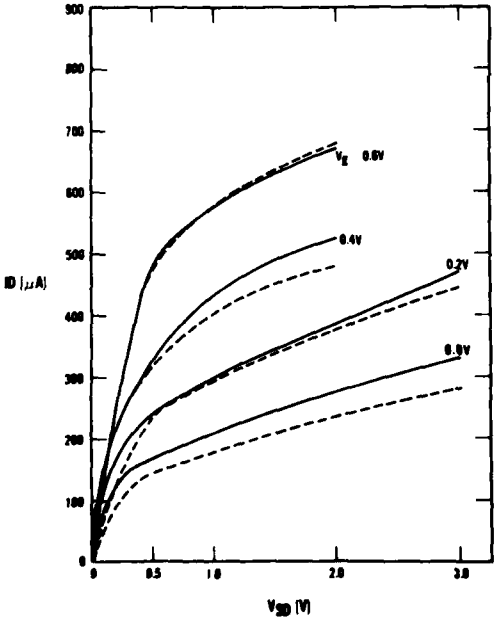
Device Modeling

The two-dimensional charge-sheet model for short-channel MOS transistors was extended to transistors of channel length down to 1 μm. The model is formulated to include the effect of channel inversion layer charge as a nonlinear integral boundary condition on the two-dimensional electrostatic fields in the transistor. This formulation allows the drain current and electrostatic potential to be computed simultaneously without including the full electron current continuity equation. This simplification results in significant increases in computational efficiency.

The simulations produced using this model have been compared with experimental measurements. Although some conver-

gence problems occur, it is possible to make useful comparisons between measured data and the two-dimensional charge-sheet model for transistors with channel lengths longer than 1.12 μm. The transition between output characteristics which look like long-channel characteristics in the saturation region and those which look like short-channel characteristics occurs for channel lengths between 3.20 and 1.89 μm.

In the accompanying figure, output characteristics computed from the model for a 1.89-μm transistor are compared with measured data. In contrast, there is no similarity between the long-channel theory of the one-dimensional charge-sheet model and the measured data for this 1.89-μm transistor; the long-channel theory fails because the effect of source-drain field-induced channel inversion is neglected. At some channel length below 1 μm, two-dimensional electrostatic effects become so large that the channel current is no longer confined to the surface of the transistor; for such devices, which are outside the range being considered here, the charge-sheet model fails.



Output characteristics for a 1.89-μm transistor. Dashed lines, 2-D theory; solid lines, measured.

Short-channel effects are greatly enhanced in these transistors due to the low dopant density in the channel, 10^{15} cm^{-3}. If the dopant density is increased, the transition to short-channel characteristics and the failure of the charge-sheet model occur at shorter channel lengths. For example, with a dopant density of 10^{16} cm^{-3}, a 0.35-μm transistor exhibits effects comparable to those of a 1.12-μm transistor of the type described here.

An important feature of this work is that the numerical solutions were obtained using general-purpose software for solving elliptic partial differential equations (PDEs). The numerical software was inspired by finite-element software of Bank and Sherman and retains most of their philosophy. With this software, it is possible to solve problems with exact solutions to test the correctness and accuracy of the codes and to determine optimal strategies and optimal values for parameters in the code. It is also possible to change easily both the physics included in the model and the geometry of the problem.

The numerical accuracy of this implementation of the charge-sheet model can greatly exceed the accuracy required for most applications. For example, to obtain 5-percent accuracy for drain current, a 146-element mesh using 10 Newton steps and a relative Newton step convergence criterion of 2 percent are sufficient. Refinement of the 146-element mesh to a 455-element mesh gives the current with a computational accuracy of 0.16 percent. [Sponsor: 2]

(C. L. Wilson, x3621, and J. L. Blue*)

Acoustic-Emission Testing

An acoustic-emission (AE) test system suitable for comparing the pull force or

*NBS Scientific Computing Division.

the flexure fatigue strength of different alloy leads or the susceptibility of surface platings to crack or to separate during flexure was developed. It has been applied to tape-bonded (TAB) integrated circuit leads and package lead frames. In use, an individual bonded lead is clamped by a microtweezer and is pulled or vibrated at a frequency of between 10 and 100 Hz, and the acoustic emission is monitored. Power for the vibration solenoid is passed through an electronic switch which is turned off by the acoustic-emission trigger unit when a bond begins to lift, lead fatigue cracks propagate, or the lead plating separates.

Lead vibration tests were carried out to compare the fatigue characteristics of 11-mm all-copper tape with thermocompression (TC)-bonded copper leads and 35-mm polyimide-based tape with tin-plated copper leads, melt-bonded to gold bumps. Such tests were usually carried out with a constant upward pull force of 50 mN and a vibration force of ±9.8 mN at 40 Hz. The microtweezer hook clamped the lead approximately 0.015 cm out from the chip. In all cases, the tin-plated leads on the 35-mm format broke within 1 to 2 s at the edge of the bump (40 to 80 vibration cycles), whereas the unplated TC-bonded leads of the 11-mm tape withstood at least 10 times as many vibration cycles before breaking at the edge of the bump. Only a few prebreak AE bursts were recorded for either type of lead. However, since a totalizer which prints AE data once each second was used for data analysis, it is possible that prebreak bursts occurred within the final second and were not separated from AE generated during the break.

It was concluded that the combination of tin plating and alloy bonding resulted in a much more brittle bond heel than that of the TC-bonded unplated copper leads. This was verified by fatiguing the tin-plated leads at their tape interface where no gold-tin alloy was present. The fatigue strength of this end of the lead (including corrections for increased line width) was as high as that of the unplated TC-bonded leads. Thus, it is concluded that the gold-tin-copper alloy had embrittled the lead at the edge of the bump. The implication is that if TAB devices are to be in plastic-encapsulated packages, the unplated copper would best withstand thermal cycling environments such as those encountered in automotive applications. TAB devices from one manufacturer's lot in each tape size were available for these tests. The purity and hardness of the leads were not known, so it is possible that other similar TAB leads may show better fatigue strength. However, considering the factor of ten difference in microfatigue strength, it appears desirable to conduct fatigue tests when determining the lead-bonding parameters (time, temperature, and force) as well as finished device suitability for encapsulation and use in extreme environments. [Sponsor: 2]

(G. G. Harman, x3621)

Production Bond Tester for TAB ICs

A prototype automatic tester has been designed for production monitoring of the bond quality of tape-bonded integrated circuits. In operation, the tape is advanced until the chip is centered in the fixture. A tool clamps the chip by pressing down on top of the bonds on two opposite sides of the chip. Another tool rises from below, exerts a vertical lifting force against the unclamped leads, and bends them upward. The acoustic emission (AE) resulting from this stress is monitored. The force applied to the leads is dependent on how close the tool is to the edge of the chip. The desired test force is experimentally determined for each device type or lead design, but is on the order of 100 mN per lead. The clamp force is then released, both tools are rotated 90 deg, and the remaining bonds are tested.

Both a trigger unit and a totalizer which cumulates all AE events above a preset threshold each second are used to assist in the interpretation of fail-

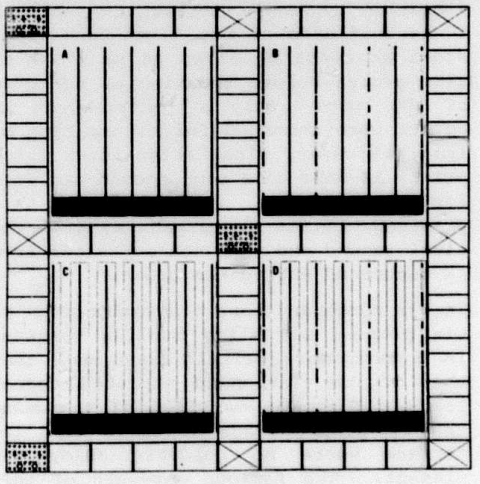
ures. The AE detector can be time-gated to be sensitive only after approximately 10 mN per lead has been applied in order to avoid any interference noise from contact or scraping. The gate window is closed after maximum force is applied.

For most effective acoustic-emission quality assurance testing of TAB bonds, the test fixture should be designed to apply a relatively high peel force; this is achieved by lifting the leads as near as practical to the edge of the chip. This system performs two functions: (1) The bonds are subjected to a preset nondestructive "lift" force. If any of them fail during the test, the AE monitor using the trigger can signal for rejection of that device. If any bonds partially lift, the resulting AE signal can be processed to reject or accept the device as desired. This test is equivalent to the nondestructive pull test that is applied to millions of wire bonds for high reliability semiconductor devices. (2) The leads are automatically "formed" or bent upward to give more lead-to-chip clearance and prepare them for outerlead bonding. Lead forming is often a required step when the chips are to be bonded face up, and so this AE-monitored bond test need not increase the number of assembly processing steps. [Sponsor:] (G. G. Harman, x3621)

Solar Cell Measurement Techniques

Preliminary laser scan measurements of the four solar cells on test pattern NBS-22 have confirmed the predictions of theoretical photoresponse curves developed for solar cells with contact fingers on the cell surface.* Test pattern NBS-22 contains four *n-p* solar cells, three of which have intentional, controlled imperfections. Cell A has no intentional defects; cell B has different length gaps in the metallization contact to the cell's top surface (but not in the metallization itself); cell C has a doubly diffused region beneath and adjacent to each metallization grid line to provide, in conjunction with the normal, singly diffused region, two values of emitter sheet resistance; and cell D has the defects of B and C combined, as shown in the accompanying figure. Surrounding each cell are 16 repetitions of a set of reference test structures fabricated by the same processes as the solar cells.

A point-by-point comparison between the measured photoresponse from the laser spot as it was scanned along a line across cell A and the predictions of the theoretical photoresponse equation verified the correctness of the photoresponse equation within the experimental accuracy. A quantitative comparison based on sheet resistance measurements from the reference test structures further confirmed the correctness of the equation. The importance of this result is that the dependence of the photoresponse on the position of the light spot relative to a metallization line may be predicted for various levels of full cell illumination. This dependence may then be separated from photoresponse variations due to cell defects independently of where the defect happens to be located.



Solar cell test pattern NBS-22.

*The theoretical development was carried out under subcontract by A. Fedotowsky and K. Lehovec of the University of Southern California.

In addition, intentionally introduced nonuniformities in sheet resistance, junction depth, and metallization contact were examined with the laser scanner, and the capability of the scanner to detect these nonuniformities was evaluated. The laser photoresponse was found to be very sensitive to changes in junction depth but relatively insensitive to abrupt changes in sheet resistance due to the averaging effect of charge collection to metallization lines on both sides of the sheet resistance change. Breaks in top metallization contact to the cell were found to be detectable if the length of the break was greater than approximately one-half of the current attenuation length in the cell which is dependent on the level of overall illumination on the cell. [Sponsor: 11] (W. F. Lankford, P. Kowalski, and H. A. Schafft, x3621)

Power Loss in Transistor Switching

It was previously shown that the skin effect in the package leads caused an interference with the standard thermal resistance measurement in hermetically sealed bipolar power transistors. Subsequent investigations have shown that the same phenomenon can cause a significant power loss to occur in the package leads of power transistors used in high frequency switching applications. The skin effect occurs in all conductors; however, it is most severe in magnetic conductors because the surface resistance increases as the square root of the magnetic permeability. The material used for package leads on hermetic packages is typically an iron-nickel-cobalt alloy, which has a thermal expansion coefficient closely matched to the sealing glass, but also has a very high magnetic permeability. Until now, the power loss at high frequency due to the magnetic properties of the package leads had not been considered.

A method was developed in which a "dummy" semiconductor package is used for measurements of the power loss of the package leads independently of the switching transistor chip housed in the package. Power loss comparisons have been made for a power MOSFET operating at 100 kHz housed in a TO-3 package. A portion of a flyback converter operating at 50-percent duty cycle at 100 kHz produced 5.8 W of power loss in the switching transistor. The power loss in the package source lead was 0.6 W, or 11 percent of the total loss. In a similar circuit built using a resistive load, it was found that 12 percent of the total loss in the transistor occurred in the source lead. As converter frequencies become higher and transistor chip efficiencies improve, package lead power losses may become very important and limit the usefulness of traditional semiconductor packages. Furthermore, passive components such as capacitors with magnetic leads will also have power losses in the leads at high frequencies. [Sponsor: 13] (D. W. Berning and D. L. Blackburn, x3621)

Second Breakdown in Power MOSFETs

A circuit has been designed and built for use in a number of different studies of the reverse-bias second breakdown (RBSB) behavior of selected different types of power transistors. The circuit makes the collector or drain load of the transistor under test appear to the transistor as an infinite inductance when the transistor is being turned off. The circuit consists of a 10-kW peak power operational amplifier that can supply a current of 10 A at a voltage of 1 kV for up to 10 ms. The circuit provides a low capacitance constant current source. As such, it permits the high speed protection circuit that is necessary for making nondestructive measurements of second breakdown (SB) to remain effective and uncompromised.

With the new circuit, transistors can be tested under conditions for which the collector voltage at turnoff reaches the reverse-bias sustaining voltage, $V_{CEX}(SUS)$, but the collector cur-

rent I_C does not decay significantly from its maximum value. The circuit is being used in a study to determine the susceptibility of bipolar devices to thermal instability during turnoff and in a study of thermal instability and SB in power MOSFETs.

Preliminary results from the latter study indicate that SB can occur in power MOSFETs. * In this study, the reverse-bias safe-operating-area test circuit, originally designed for nondestructive SB tests on bipolars, has been successfully used to nondestructively test power MOSFETs for SB. Some of these devices experience SB with a nominal 1-mH inductance in the drain circuit, whereas others have required the use of the "infinite-inductance" circuit to experience SB. The SB behavior of these devices is not influenced by the magnitude of the "off bias" applied to the gate. The drain voltage waveform at the onset of SB looks identical to the collector voltage waveform of bipolar devices; i.e., it collapses in about 10 ns to approximately 100 to 200 V. The SB characteristics are extremely repeatable (within the approximately 10-V, 0.2-A measurement resolution of the system) for successive excursions into SB. [Sponsors: 2,13] (D. W. Berning and D. L. Blackburn, x3621)

Radiation Effects on Power MOSFETs

Recent advances in power MOSFET technology have opened new application areas for these devices. As majority-carrier devices without minority-carrier charge storage effects of bipolar transistors, power MOSFETs are capable of faster switching speeds than power bipolar transistors. Also, a negative temperature coefficient of carrier mobility greatly decreases the potential for thermal runaway, second breakdown, and current hogging in power MOSFETs as compared to bipolar devices. However, the effects of radiation on power MOSFETs and effects of device design on radiation susceptibility have not yet been well established. Data on the effects of gamma irradiation on threshold voltage and the effects of a mixed gamma-neutron environment on breakdown voltage have been reported in the literature. Research has been initiated to study the effects of radiation on the on-resistance (R_{on}) of vertical double-diffused power MOS (VDMOS) transistors. It is expected that radiation damage will primarily manifest itself through shifts in threshold voltage due to ionizing radiation exposure and changes in the resistivity of the lightly doped *n*-type epitaxial layer due to neutron exposure.

Data were obtained on the effects of both gamma and neutron environments on this parameter, and a simple model to predict the effects of radiation on on-resistance is being tested. Preliminary results of measurements on a variety of VDMOS devices before and after neutron irradiation to a fluence of 1×10^{14} cm^{-2} (energy > 10 keV) suggest that the increase in R_{on} with neutron irradiation is greater for high-voltage devices (which have lower dopant density in the epitaxial layer). For example, for devices with breakdown voltage of about 450 V (dopant density $\sim 2 \times 10^{14}$ cm^{-3}), the resistance increased by about a factor of 13; for devices with breakdown voltage of about 350 V (dopant density $\sim 4 \times 10^{14}$ cm^{-3}), the on-resistance increased by about a factor of 6; and for devices with breakdown voltage of about 100 V (dopant density $\sim 3 \times 10^{15}$ cm^{-3}), no increase in on-resistance was evident. These results are consistent with the published predictions of Buehler on the increase of silicon resistivity with neutron fluence as a function of initial resistivity. A full analysis is now underway. [Sponsor: 2]

(T. C. Robbins,* D. L. Blackburn, x3621, and K. F. Galloway, x3786)

Federal IC Processing Facilities

The Federal Government maintains a number of microelectronics processing fa-

*Department of Defense, Ft. George G. Meade, Maryland.

cilities for a diversity of purposes, including research, maintenance of technical capabilities, and prototype development. Many of these facilities have equipment which can be made available to qualified university research workers, have projects which can involve university faculty and students, and have staff which would welcome collaborative opportunities with university personnel. An informal telephone survey was undertaken to provide data to the university community on the work of nine Federal microelectronics facilities. Information relating to the equipment at hand that might be available for collaborative efforts, the general mission, and the general attitudes at these facilities toward cooperation with university personnel on research or part-time employment has been summarized in tables. A report of the survey results was presented at the 1981 University/Government/Industry Microelectronics Symposium. Copies of this information may be obtained on request. (K. F. Galloway, x3786, and M. C. Peckerar†)

Recent Publications ...

Forman, R. A., Larrabee, R. D., Myers, D. R., Phillips, W. E., and Thurber, W. R., Processing Effects on the Electrical and Optical Properties of Sulfur-Related Defect Centers in Silicon and Similarities to the Oxygen Donor, *Defects in Semiconductors*, J. Narayan and T. Y. Tan, Eds., pp. 79-84 (North Holland, New York, 1981).

*Lehovec, K., and Fedotowsky, A., Solar Cell Mathematical Analysis and Computer Simulation, NBS-GCR-80-285 (January 1981).

Sawyer, D. E., Kessler, H. K., Russell, T. J., Lankford, W. R., and Schafft, H. A., Measurement Techniques for Solar Cells, Annual Report, December 15, 1978 to December 14, 1979, NBSIR 80-2181 (January 1981).

Scace, R. I., Semiconductor Technology for the Non-Technologist, NBSIR 81-2197 (January 1981).

Geist, J., and Lowney, J. R., Effect of Band-Gap Narrowing on the Built-In Electric Field in n-Type Silicon, *J. Appl. Phys.* 52, 1121-1123 (February 1981).

Bullis, W. M., Advancement of Reliability, Processing, and Automation for Integrated Circuits with the National Bureau of Standards (ARPA/IC/NBS), NBSIR 81-2224 (March 1981).

Mitchell, M. A., and Linholm, L. W., *Semiconductor Measurement Technology:* Test Patterns NBS-28 and NBS-28A: Random Fault Interconnect Step Coverage and Other Structures, NBS Spec. Publ. 400-65 (March 1981).

Novotny, D. B., Photoresist Sensitometry and Exposure Modeling, *Solid State Technology* 24 (3), 83-92 (March 1981).

*Linares, L. C., and Li, S. S., An Improved Model for Analyzing Hole Mobility and Resistivity in p-Type Silicon Doped with Boron, Gallium, and Indium, *J. Electrochem. Soc.* 128 (3), 601-608 (March 1981).

Blackburn, D. L., Power Transistor Switching Characterization, NBSIR 81-2204 (April 1981).

Buehler, M. G., and Perloff, D. S., Microelectronic Test Chips and Associated Parametric Testers: Present and Future, *Semiconductor Silicon/1981*, H. R. Huff, R. J. Kriegler, and Y. Takeishi, Eds., pp. 859-867 (ECS, Pennington, New Jersey, May 1981).

Linholm, L. W., Mattis, R. L., Frisch, R. C., and Reeves, C. P., Characterizing and Analyzing Critical Integrated Circuit Process Parameters, *Semiconductor Silicon/1981*, H. R. Huff, R. J. Kriegler, and Y. Takeishi, Eds., pp. 906-920 (ECS, Pennington, New Jersey, May 1981).

Berning, D. W., and Blackburn, D. L., The Effect of Magnetic Package Leads on the Measurement of Thermal Resistance of Semiconductor Devices, *IEEE Trans. Electron Devices* ED-28, 609-611 (May 1981).

Carver, G. P., and Cullins, W. A., *Semiconductor Measurement Technology:* A Manual Wafer Probe Station for an

†Naval Research Laboratory.

*Reports of contract research.

Integrated Circuit Test System, NBS Spec. Publ. 400-68 (May 1981).

Carver, G. P., Mattis, R. L., and Buehler, M. G., Microelectronic Test Patterns NBS-12 and NBS-24, NBSIR 81-2234 (May 1981).

Lankford, W. F., Kowalski, P., and Schafft, H. A., Laser Scanning Measurements on Solar Cell Test Pattern NBS-22, NBSIR 81-2260 (May 1981).

Schafft, H. A., Ruthberg, S., and Cohen, E. C., *Semiconductor Measurement Technology:* ARPA/NBS Workshop V. Moisture Measurement Technology for Hermetic Semiconductor Devices, NBS Spec. Publ. 400-69 (May 1981).

Thurber, W. R., Mattis, R. L., Liu, Y. M., and Filliben, J. J., *Semiconductor Measurement Technology:* The Relationship Between Resistivity and Dopant Density for Phosphorus- and Boron-Doped Silicon, NBS Spec. Publ. 400-64 (May 1981).

Larrabee, R. D., Thurber, W. R., and Bullis, W. M., Electrical Parameters of Extrinsic Silicon, *Circuits Manufacturing* 21 (5), 92-100 (May 1981).

Buehler, M. G., and Linholm, L. W., Toward a Standard Test Chip Methodology for Reliable, Custom Integrated Circuits, *Proc. 1981 Custom Integrated Circuits Conf.*, Rochester, New York, May 11-13, 1981, pp. 142-146.

Galloway, K. F., and Peckerar, M. C., Informal Survey of Federal Government Microelectronics Processing Facilities, *Proc. 4th Biennial University/Government/Industry Microelectronics Symp.*, Mississippi State University, May 1981, pp. III-24 - III-30.

*Vasquez, R. P., Klein, J. D., Barton, J. S., and Grunthaner, F. J., Application of Maximum Entropy Spectral Estimations to Deconvolution of XPS Data, *J. Electron Spectrosc.* 23, 63-81 (May 1981).

Publications in Press ...

Baghdadi, A., and Forman, R. A., Tertiary Interferograms in Fourier Transform Spectroscopy, *Appl. Spectrosc.*

*Reports of contract research.

Bennett, H. S., and Lowney, J. R., Effect of Donor Impurities on the Density of States Near the Band Edge in Silicon, *J. Appl. Phys.*

Berning, D. W., Use of Vacuum Tubes in Test Instrumentation for Measuring Characteristics of Fast High Voltage Semiconductor Devices, *IEEE Trans. Instrum. Meas.*

Buehler, M. G., and Linholm, L. W., The Role of Test Chips in Coordinating Logic Design and Layout Aids for VLSI, *Proc. 2nd Cal. Tech. Conf. on VLSI*, Pasadena, California, January 1981.

Bullis, W. M., and Nyyssonen, D., Optical Linewidth Measurements on Photomasks and Wafers, Chapter in *Microstructure Science and Engineering*, Vol. 3, Norman G. Einspruch, Ed. (Academic Press, New York).

Bullis, W. M., Trends in Integrated Circuit Metrology, *EDN Magazine.*

Candela, G. A., Galloway, K. F., Liu, Y. M., and Fine, J., Measurements of the Interlayers Between Al and SiO_2 Using Ellipsometric, Capacitance-Voltage, and Auger Electron Spectroscopy Techniques, *Thin Solid Films.*

Forman, R. A., Myers, D. R., and Bell, M. I., Comments on "Raman Scattering from Boron-Implanted Laser-Annealed Silicon" by H. Engstrom and J. B. Bates, *J. Appl. Phys.*

Harman, G. G., The Use of Acoustic Emission as a Test Method for Microelectronic Interconnections and Joints, *Proc. 2nd Internat. Conf. Loten und Schweissen in Der Elektronik*, Munich.

*Lin, J. F., Li, S. S., Linares, L. C., and Teng, K. W., Theoretical Analysis of the Hall Factor and Hall Mobility in *p*-Type Silicon, *Solid-State Electronics.*

Linholm, L. W., *Semiconductor Measurement Technology:* The Design, Testing, and Analysis of a Comprehensive Test Pattern for Measuring CMOS/SOS Process Performance and Control, NBS Spec. Publ. 400-66.

Lowney, J. R., Kahn, A. H., Blue, J. L., and Wilson, C. L., Disappearance of Impurity Levels in Silicon and Ger-

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☐ Document describes a computer program; SF-185, FIPS Software Summary, is attached.

11. ABSTRACT (A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here)

This report provides information on the current status of NBS work on measurement technology for semiconductor materials, process control, and devices. Emphasis is placed on silicon and silicon-based devices. Highlighted activities include newly issued resistivity SRMs, characteristics of sulfur-related deep levels in silicon, photoluminescence of indium-doped silicon, effect of tertiary interferograms on Fourier transform spectroscopy, design information for a set of wafer optical linewidth standards, modeling of short-channel MOS transistors, acoustic-emission testing of tape-bonded ICs, laser scanning of a solar cell test pattern, power loss of transistor leads during fast switching, and second breakdown and radiation effects in power MOS transistors. Brief descriptions of an upcoming linewidth measurement seminar and a survey of Federal IC processing facilities are given. In addition, recent publications and publications in press are listed. The report is not meant to be exhaustive; contacts for obtaining further information are listed.

12. KEY WORDS (Six to twelve entries; alphabetical order; capitalize only proper names; and separate key words by semicolons)

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manium Due to Screening, *J. Appl. Phys.*

Mitchell, M. A., Linholm, L. W., Russell, T. J., and Carver, G. P., Electrical Test Structures for Characterization and Control of Microelectronics Processing, *Proc. Microelectronic Measurements Technology Workshop*, San Jose, California, March 23, 1981.

Myers, D. R., Wilson, R. G., and Comas, J., Effect of Silicon Dioxide Surface Layers on Boron Profiles for Accurately Aligned Implants Into <110> Silicon, *J. Appl. Phys.*

Phillips, W. E., Improved Thermometry for Deep-Level Measurements, *J. Physics E.*

Ruthberg, S., Graphical Solution for the Back Pressurization Method of Hermetic Test, *IEEE Trans. Components, Hybrids, and Manufacturing Tech.*

Schafft, H. A., Measurement Development Needs for Photovoltaics and Recommended Responses, NBSIR 80-2126.

*Schwarz, S. A., Helms, C. R., Spicer, W. E., and Taylor, N. J., *Semiconductor Measurement Technology:* The Capabilities and Limitations of Auger Sputter Profiling for Studies of Semiconductors, NBS Spec. Publ. 400-67.

Wilson, C. L., and Blue, J. L., Semiconductor Device Simulation, *Proc. Conf. Elliptic Problem Solvers*, Sante Fe, New Mexico, June 30-July 2, 1980.

*Reports of contract research.

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